Remarks:

Applicant appreciatively acknowledges the Examiner's confirmation of receipt of applicant's claim for priority and certified priority document under 35 U.S.C. § 119(a)-(d).

Reconsideration of the application is requested.

Claims 1-16 are currently pending in the present application. Claims 1, 5 - 9, 14 and 15 have been amended herein to more clearly set forth the claimed inventions.

On page 2 of the above-named Office Action, the Abstract of the Disclosure was objected to as failing to comply with the proper format. Applicant has amended herein the Abstract of the Disclosure of the present application to remove any handwritten marks and to ensure that the abstract appears in narrative form, in a single paragraph, on a separate sheet and is between 50 and 150 words in length.

In paragraph 2 on page 2 of the action, the specification was objected to because of a number of informalities involving, in part the term "programming potential" used in the specification. Additionally, claims 1, 9, 10 and 16 were rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the enablement requirement. Further,

claims 1 - 16 were rejected under 35 U.S.C. § 112, second paragraph as allegedly being indefinite. Finally, Claims 1 - 16 were rejected as allegedly being anticipated by a number of references. Applicant respectfully traverses the above rejections.

I. Applicant's specification defines the terms "programming potential" and "no potential" and their meaning in that context is clear from a review of the application and its accompanying drawings.

In the Office Action, it is asked that Applicant explain the term "**programming potential**" used in the specification. Additionally, the use of the term "**no potential**" in the claims is questioned. By the following explanation, supported by the specification and the logical circuit analysis, Applicant will clear up any confusion relating to the above terms.

In the present application, "**programming potential**" is a fixed potential supplied by a voltage source, e.g. by a supply voltage which, as shown in the depicted embodiments, is the ground potential. This is supported in Applicant's specification at page 13, lines 14 - 20. See also, page 13, line 22 - page 14, line 2, where the terms **programming potential** and ground potential are used in a manner as to denote interchangeability.

On the other hand, "**no potential**" is used to denote exactly what it says, the absence of an applied potential (i.e. neither the source voltage VDD or the **programming potential**/ground potential). The term "**no potential**" applied to a node means that the respective node is not fixed to a specific potential, but rather, a high impedance is applied which allows the voltage at the respective node to float dependent on other components of the circuit. This is clear in view of the figures wherein the switching elements apply the ground potential to the nodes K1 and K2 when closed and apply "**no potential**" (i.e. a high impedance floating node) at K1 and K2, respectively, if the switching elements 8 and 9 are opened. From page 16 of the application, lines 5 - 11, and Fig. 1, it can be seen that the term "**no potential**" is used to describe the state when one of the switching elements 8, 9 is inhibited and drops out of the circuit.

Addressing the objection to the specification on page 2 of the Office Action, the circuit of Fig. 1 operates as described at page 16 of the current application, lines 1 - 20, which states:

> "The flip-flop circuit 1 described above is able to accept a data signal at the data input 3 into the data acceptance unit 5 in the event of a low level of the clock signal CLK and to write it to the storage element 4 in the event of a high level of the clock signal CLK. The process of writing to the storage element 4 is effected through the first switching element 8 and the second switching element 9, only one of the two

> switching elements 8, 9 being activated, while the respective other switching element is inhibited and, consequently, no potential is applied to the node K1, K2 of the feedback loop that is present at the switching element. The node K1, K2 of the feedback loop that is connected to the activated switching element 8, 9 is pulled to a low level corresponding to the ground potential GND and is inverted by the corresponding inverter circuit 6, 7 so that a high level is present at the respective other node K1, K2 of the feedback loop. The two nodes K1, K2 of the feedback loop of the storage element 4 are available as outputs of the flip-flop Q, QN, the first node K1 corresponding to the non-inverted output Q and the second node K2 corresponding to the inverted output QN."

As such, it can be seen, that the states of the switching elements 8, 9 connected to the storage unit at nodes K1 and K2 are always either "**no potential**" (floating) or "**programming potential**" (connected to ground, in the present embodiment).

One particular example of the operation of the circuit of Fig. 1 will now be given to demonstrate the application of the **programming potential**, and of **no potential** to that circuit. The high output at Q or QN is supplied by the power supply VDD to the storage unit 4, as a result of the feedback loop between the inverters 6 and 7 when one of the switching elements 8, 9 is tied to ground and the other is inhibited (i.e. an open-circuit). In the present example, if the input D is high, and the clock is low, an inverted representation of D is applied to T2 and a non-inverted representation of D is applied to T4 using inverting sections 11 and 10, respectively. When the clock goes high, the inverter stages

10 and 11 are cut off, but the potential at the gate terminals of the transistors T2 and T4 remain at their specific potentials. This occurs because the system is not static and, at the higher frequencies at which the circuits are operated, the capacitances of the gates and signal lines have to considered.

Discussing these capacitances in more detail, when the clock is low, the respective signals are applied on the transistors T2 and T4, one is high and one is low. When the clock transitions from low to high, the power supply from the inverters 10, 11 is cut, but, if the output node of inverter 10 was high it remains high because of the gate capacitance of the transistor T2 and because transistor T5 is open and the node cannot be discharged. If the output of the inverter 10 was low, the gate of transistor T5 was probably high and T5 is, therefore, conductive, keeping the gate of transistor T2 low.

Similarly, if the output node of inverter 11 was high when the clock transitioned from low to high, it remains high for a moment because of the gate capacitance of transistor T4 and because transistor T8 is open and the node cannot be discharged. If the output of the inverter 11 was low the gate

of transistor T8 was probably high making T8 conductive, holding the gate of transistor T4 low.

Due to the above described circuit function and gate capacitances, after the clock transitions from low to high, the output nodes of the inverters 10 and 11 still maintain their respective potentials for at least a short time, which is sufficient to close the respective switching element 8, 9 and connect the respective node K1 or K2 to ground. The short time of the potential maintained at the outputs of the inverters is determined by parasitic effects like leakage and the like. In an ideal circuit, the short time would be infinite, because there is no sink for the charge potential to be discharged. However, in the presently described circuits the short time in which the switching element 8 or 9 is closed is sufficient to write to the storage element.

Returning to the discussion of the circuit, once the clock is high, the transistors T3 and T1 are turned on. In the present example, due to the lingering potential at one or the other of node 11, the switching element 9 (with T3 and T4 high) is closed, tying the node K2 to the **programming potential** (ground), while the switching element 8 is inhibited (T2 is turned off while T1 is high). As such, the switching element 8 is floating and providing **no potential** to the storage unit

4, thus having no effect on inverters 6 and 7. This is easily determined from reviewing the circuit of the present preferred embodiment and its description, and was apparent to the Examiner, who in the Office Action, at page 2, lines 17 - 18, stated,

> "According to the connection to the switching elements (8) and (9), no high potential level can be generated by the switching elements (8) and (9)."

Because of the above states of the switching elements 8 and 9, node K2 goes to ground potential and the output Q of the inverter 7 goes to VDD the storage unit 4. As a result of the feedback loop in the storage unit 4 and of the lack of any potential at K1, the input to the inverter 6 goes high, and its output QN is low. This output is locked into the storage unit 4 until at least the next time the clock goes high. Had the data signal D been low during the low clock period of the present example, it can be seen that upon the clock going high, the switching element 9 would have provided **no potential** to the storage unit 4 and the switching element 8 would have provided the **programming potential** (i.e. ground level). In this case, because of the feedback loop between the inverters 6 and 7, Q would be low and QN would be high.

It can be seen that the circuit of Fig. 2 operates in a similar manner with provision being made for the addition of an activation signal E.

In view of the above discussion, Applicant believes that the terms "**programming potential**" and "**no potential**" are clear to a person of ordinary skill in the art and are, further, defined in the specification and that the objections to the specification and claims based on the use of those terms should be withdrawn.

II. Applicant's claims are enabling and definite under 35 U.S.C. § 112 first and second paragraphs.

On page 2 of the Office Action, claims 1, 9, 10 and 16 were rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the enablement requirement. More specifically, the Office Action states:

> "In claim 1, the recitation 'said data acceptance unit being **adapted to** allocate, dependent upon the data signal present and the **clock signal** present, **predetermined programming potential** either to said first input or to said second input and to apply **no potential** to the respective other input of said first and second inverter circuits…' is non enable [sic] because in order to have data (D) transferred to the storage unit, inverters (10) and (11) must be enabled by a low clock (CLS). But when the clock is low, transistors (T1) and (T3) of switching elements (8) and (9) are turned off. Thus, data D) [sic] or a voltage derived fron [sic] data (D) cannot be forwarded to the storage unit (4). It is also unclear what the "no potential" and the "predetermined potential" are meant by. The analysis is true for claim 16.
> Claims 9 and 10 are non-enable[sic] because according to figure 1, clock (CLK) needs to be at low potential level in order to forward data (D) to the switching elements (8) and (9). With the low level of the clock signal, switching elements (8) and (9) are inhibited thus, no data can be stored in the storing device."

Claims 1 - 16 were rejected under 35 U.S.C. § 112, second paragraph on pages 3 - 6 of the Office Action for the reasons for which the specification was objected, as well as some additional reasons that will be pointed out individually herebelow. Applicant respectfully traverses these rejections of the present claims.

On pages 3 and 4 of the Office Action, claims 1-16 were rejected based on the "**no potential**", the circuit function and the term "adapted" being used in the claims.

Claim 1 has been amended to remove the term "adapted" from the claim. Further, as described above in section I, that section being incorporated herein, the terms "**programming potential**" and "**no potential**" are defined in the specification such that **programming potential** is a desired voltage potential, and in the present embodiments is defined as the ground potential. See page 13, lines 14 - 20. This definition can also be seen from reviewing the operation of the circuit in light of the description in the specification and the figures. Similarly, as discussed above, **no potential** is defined in the specification, as well as given its plain meaning of applying no potential, but rather a high impedance element, to the circuit. This is supported in the present application at page

16, lines 5 - 11 of the present application and from a review of the figures in light of the description in the specification. As such, Applicant believes that the terms **programming potential** and **no potential** used in the present claims are enabling and asks that any objection to them, or rejection based upon those terms, be withdrawn.

Additionally, as explained above and incorporated herein, when the clock is low, D and inverted D are supplied to T2 and T4, respectively. When the clock goes high, the inverter stages 10 and 11 are cut off, but the potential at the gate terminals of the transistors T2 and T4 (D and DN) remain at their specific potentials for a long enough period to switch the switching elements, due to gate capacitance. The clock going high also turns on transistors T1 and T3. Based upon the state of D, one of the switching elements 8, 9 goes to ground potential, while the other is removed from the circuit, providing **no potential** to its respective node K1, K2. See page 16, lines 1 - 5; page 17, lines 17.

Further, on page 4 of the Office Action, regarding claims 2 - 11, Applicant was asked to point out the first switching element, second switching element, first level, second level of the clock signal, first level and second level of the data signal and the first and second partially clocked inverters.

It is believed that the above discussions explained each of these limitations obviating the objection to claims 2 - 11. Note that the first and second partially clocked inverters, not discussed as such herein, are defined in the specification as the clocked inverter sections 10 and 11.

Also on pages 4 - 5 of the Office Action, claims 5, 6 and 9 were rejected because of the term "given", used in those claims. Claims 5, 6 and 9 have been amended to better clarify what is meant in those claims.

Further on page 4 of the Office Action, claims 7 and 8 were rejected due to the both terms "no altered potential" and "non-inverted data signal" being used. In those claims, the non inverted data signal mentioned, is the one that is output from the second partially clocked inverter stage 11. Claims 7 and 8 have been amended to better clear up their meanings.

On page 5 of the Office Action, claim 12 was rejected based on various terms, including "**no potential**". It is believed that these issues were addressed in Section I above. Further, the deactivation signal is applied at E in Fig. 2 (input 21). claim 12 makes clear that it is the first partially clocked gate that applies the ground potential to the first switching element in the event of a deactivated activation signal, it is

not applied by signal, itself. The first partially clocked gate referenced is in Fig. 2 and includes at least one element not recited in the description of the first partially clocked inverter of claim 5. Although the first partially clocked inverter of claim 5 may apply a ground potential to the first switching element in the event of a deactivated activation system, claim 5 does not require it. As such, in at least this respect, the first partially clocked inverter of claim 5 and the first partially clocked gate of claim 12 are different elements, the latter reciting more than is required by the structure of the former.

On page 6 of the Office Action, claim 13 was rejected based on a question regarding what data signal is present at the gate of the transistor in the switching element when the clock goes high. As discussed herein, based on the gate capacitances and the open paths to ground, the nodes supplying the data to the switching elements maintain their levels when the clock first goes high. As such, it is believed that claim 13 is descriptive and definite as previously presented.

Further, claims 14 and 15 have been amended to add a comma to better clarify the sentence structure and address the rejection of those claims on page 6 of the Office Action.

It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, first and second paragraphs. As such, it is believed that claims 1 - 16 are properly enabled and definite and in condition for allowance.

III. Applicant's claims are patentable over the cited art.

In the Office Action, claims 1 and 16 were rejected as allegedly anticipated under 35 U.S.C. § 102(b) by U. S. Patent No. 6,445,217 to Kojima et al. ("**KOJIMA**"). Claims 1 - 10 were rejected as allegedly anticipated under 35 U.S.C. § 102(b) by U. S. Patent No.6,232,810 to Oklobdzija et al. ("**OKLOBDZIJA**"). Claims 1 and 11 - 15 were rejected s allegedly anticipated under 35 U.S.C. § 102(e) by U. S. Patent No.6,720,813 to Yee et al. ("**YEE**"). Claims 1 - 10 and 16 were further rejected as allegedly anticipated under 35 U.S.C. § 102(b) by Japanese Reference No. 10093397 ("**JAPANESE REFERENCE**"). Applicant respectfully traverses the above cited rejections of the claims.

A. Applicant's independent claims 1 and 16 require, among other limitations, a data acceptance unit that provides a programming potential to one input of the storage unit and no potential to the other input of the storage unit.

Applicant's independent claims 1 and 16, require, among other limitations, the following:

> a data acceptance unit having a first switching element and a second switching element;
>
> a storage unit having first and second inverter circuits connected in a feedback loop;
>
> wherein the data acceptance unit allocates, dependent upon the data signal present and the clock signal present , a predetermined programming potential either to said first input or to said second input and no potential to the respective other input of said first and second inverter circuits

As described above in great detail in section I, that discussion incorporated herein, one particular embodiment of the circuit operates, based on the clock (CLK) and data signal (D), to tie one switching element 8, 9 to the predetermined **programming potential** (ground, in the present example), thus tying one input of the storage unit to ground, while the other switching element 8, 9 provides **no potential** at all to the other input of the storage unit. This is clearly set forth in the language of the independent claims cited above, and fully supported in the specification.

The subject matter of Applicant's claims has the advantage that no interactions can occur between the input of the first inverter circuit and the input of the second inverter circuit which form the storage unit.

As will be shown herebelow, none of the applicable, cited references teach or suggest the claimed feature of Applicant's invention.

B. The KOJIMA reference fails to teach or suggest a data acceptance unit that provides a predetermined programming potential to one input of a storage unit and no potential to the other input, based on the state of the clock and data signals.

Applicant believes that the **KOJIMA** reference neither teaches, nor suggests, the particularly claimed data acceptance unit that allocates, depending upon the data signal and clock signal, a predetermined **programming potential** to one of the storage inputs and **no potential** at all to the other storage unit input.

Rather, the circuit of **KOJIMA** uses two transmission gates (i.e., 630 and 632 of Fig. 6) which are switched depending on the clock signal and which applies a voltage level depending on the data signal to **each** of the first and second inputs of the storage unit. In **KOJIMA** there are only two possibilities: first, the transmission gates are both closed so that **no potential** is applied to the first **and** second input of the storage unit, and secondly, both of the transmission gates are switched on so that **two** potentials representative of the differential data, i.e. a high potential **and** a low potential, derived from the data signal are applied to the first and

second inputs of the storage unit. See, column 6, lines 1 - 18.

As such, **KOJIMA**, lacks Applicant's particularly claimed data acceptance unit adapted to apply a predetermined **programming potential** to one of the storage unit inputs, **while** applying **no potential** to the other storage unit input. In view of this, it is believed that Applicant's independent claims 1 and 16, and all claims depending therefrom, are patentable over **KOJIMA**.

C. The OKLOBDZIJA reference fails to teach or suggest a data acceptance unit that provides a predetermined programming potential to one input of a storage unit and no potential to the other input, based on the state of the clock and data signals.

As with **KOJIMA**, among other limitations of Applicant's claims, **OKLOBDZIJA**, fails to teach or suggest Applicant's particularly claimed data acceptance unit adapted to apply a predetermined programming potential to one of the storage unit inputs while applying **no potential** to the other storage unit input.

In **OKLOBDZIJA,** the first and second logic blocks 34, 36, pointed to in the Office Action as allegedly representing Applicant's data acceptance unit, do not function as required by Applicant's claims. At no time does one of the logic blocks 34, 36 apply a potential to one input of the storage

block 32 **while** the other logic block 34, 36 applies **no potential** (i.e., a high impedance), so that the voltage level at the respective input is not affected by the data acceptance unit. The logic blocks 34, 36 are both "inactive" (output a high impedance state) **at the same time, under the same condition**, when set signal /S and the reset signal /R are both high. See, column 3, lines 30 - 45 of **OKLOBDZIJA.** Otherwise, when /S is high and /R is low, the output Q of logic block 34 is low. Col. 3, ll. 28 - 30. Under the same conditions, /Q output of logic block 36 is high. Col. 3, ll. 36 - 39. When the /S input is low and the /R input is high, the states of the logic blocks 34 and 36 switch. See, column 3, lines 25 - 27 and lines 39 - 41. As such, like **KOJIMA**, the logic blocks 34, 36 of **OKLOBDZIJA** are in the first case, either **both** output **no potential** when /S and /R are both high or **both** simultaneously output some potential, one high and the other low, when /S and /R are not both high. See also the description of the circuit operation, column 4, line 58 - column 5, line 33.

In view of this, it is believed that Applicant's independent claims 1 and 16, and all claims depending therefrom, are patentable over **OKLOBDZIJA**.

D. The JAPANESE REFERENCE fails to teach or suggest a data acceptance unit that provides a predetermined

programming potential to one input of a storage unit and no potential to the other input, based on the state of the clock and data signals.

The **JAPANESE REFERENCE** appears to function like that of **KOJIMA** and **OKLOBDZIJA** and **not** like Applicant's invention of independent claims 1 and 16. For example, at low clock CLK, both transistor pairs 4,5 and 6,7 (pointed to in the Office Action as allegedly being Applicant's switching elements) are turned off because of the low signal to the gates of transistors 5 and 7. When the clock CLK is high, it appears that the transistor pairs, 4,5 and 6,7 both output a voltage potential (either high or low) based upon the state of D.

As such, the **JAPANESE REFERENCE** also lacks Applicant's particularly claimed data acceptance unit adapted to apply a predetermined **programming potential** to one of the storage unit inputs, **while** applying **no potential** to the other storage unit input. In view of this, it is believed that Applicant's independent claims 1 and 16, and all claims depending therefrom, are patentable over the **JAPANESE REFERENCE**.

E. The YEE reference is not an applicable 102(e) reference, as it was filed after Applicant's priority date.

On page 8 of the above-identified Office action, claims 1 and 11 - 15 have been rejected as allegedly being fully anticipated by **YEE**.

Applicant respectfully notes that **YEE** has a United States filing date of March 17, 2003. See 35 U.S.C. § 102(e). As set forth in the Declaration of record, the instant application claims international priority of the German Application No. 102 50 869.0, filed October 31, 2002, under 35 U.S.C. § 119. Pursuant to 35 U.S.C. §§ 119, 120, and 363, Applicant is entitled to the priority date of the German application. See MPEP §§ 201.13 and 1895. Thus, the instant application predates **YEE** by more than three months. Because **YEE** was filed after the priority date of the instant application, applicant respectfully believes that **YEE** is unavailable as prior art.

Applicant acknowledges that perfection of priority can only be obtained by filing a certified English translation of the German priority application. See 35 U.S.C. § 119. Concurrent herewith, applicant has filed a Claim for Priority including both a certified copy of German application 102 50 869.0 and a certified English translation of same. Accordingly, applicant respectfully believes that priority has been perfected and **YEE** is unavailable as prior art. Therefore, applicant

respectfully submits that the Section 102 rejection on page 8 of the Office action is now moot.

F. Even if taken in combination Kojima, OKLOBDZIJA, the JAPANESE REFERENCE and YEE cannot be combined to render Applicant's claimed invention obvious.

As **KOJIMA**, **OKLOBDZIJA** and the **JAPANESE REFERENCE** all fail to teach the same limitations of Applicant's claims, among others, and since **YEE** is not a citable reference, the cited references cannot, in combination be used to teach Applicant's claimed invention.

In view of the foregoing, it is believed that Applicant's independent claims 1 and 16, and all claims depending therefrom, are patentable over the cited references.

V. Conclusion

In view of the foregoing, reconsideration and allowance of claims 1-16 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Additionally, please consider the present as a petition for a one month extension of time, and please provide a one month extension of time, to and including, October 29, 2004 to respond to the present Office Action.

The extension fee for response within a period of 1 month pursuant to Section 1.136(a) in the amount of $110.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

For Applicant

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